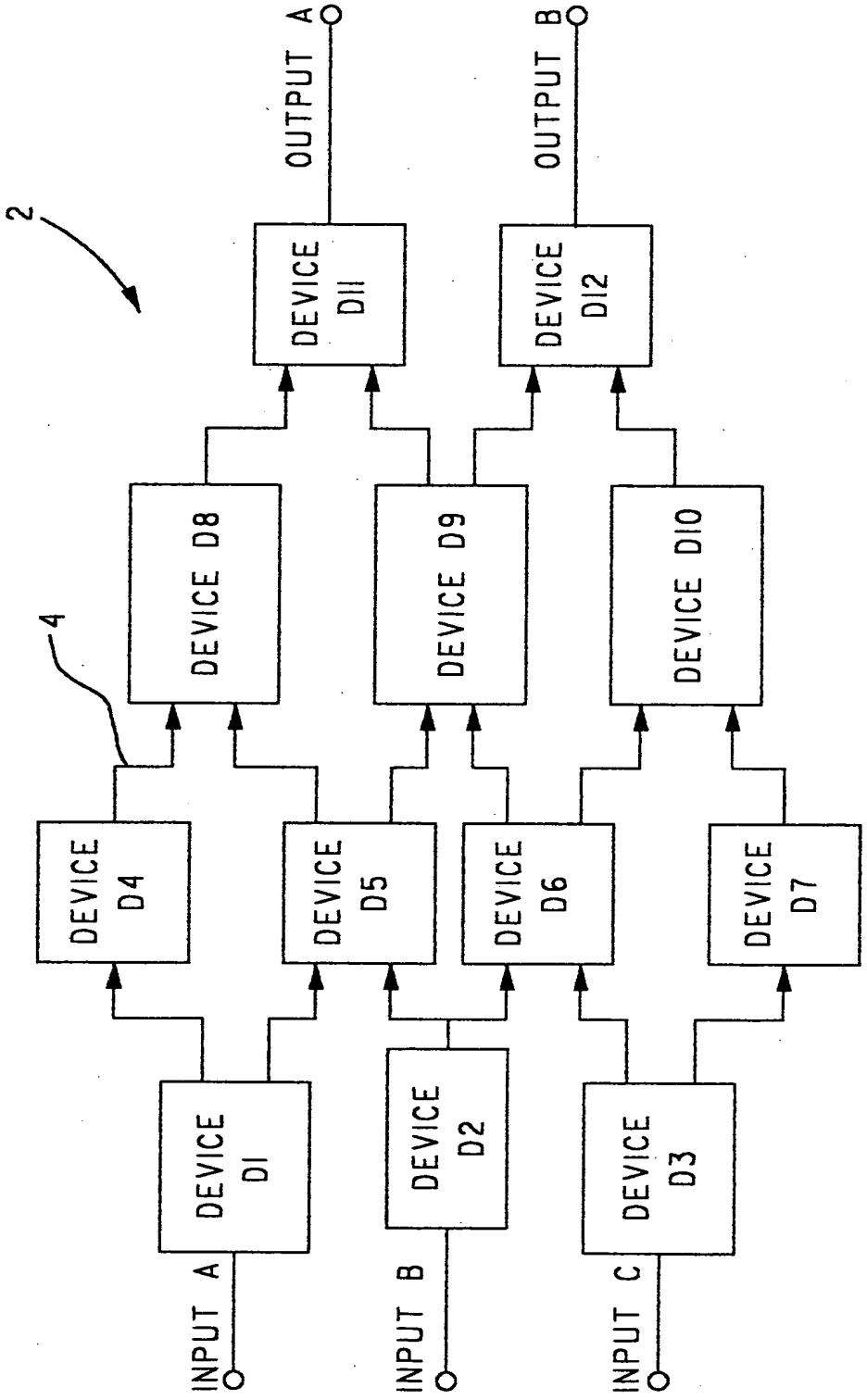
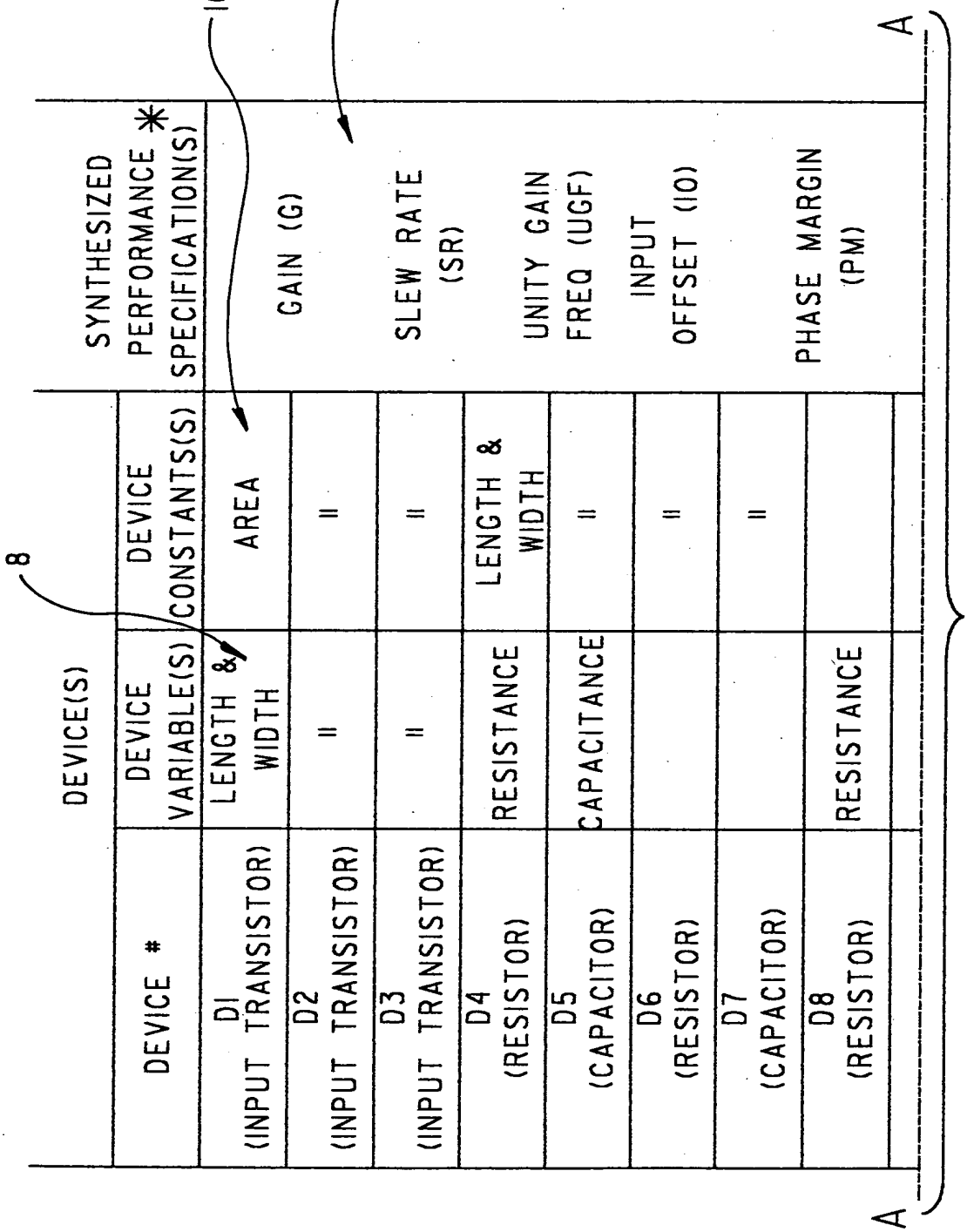
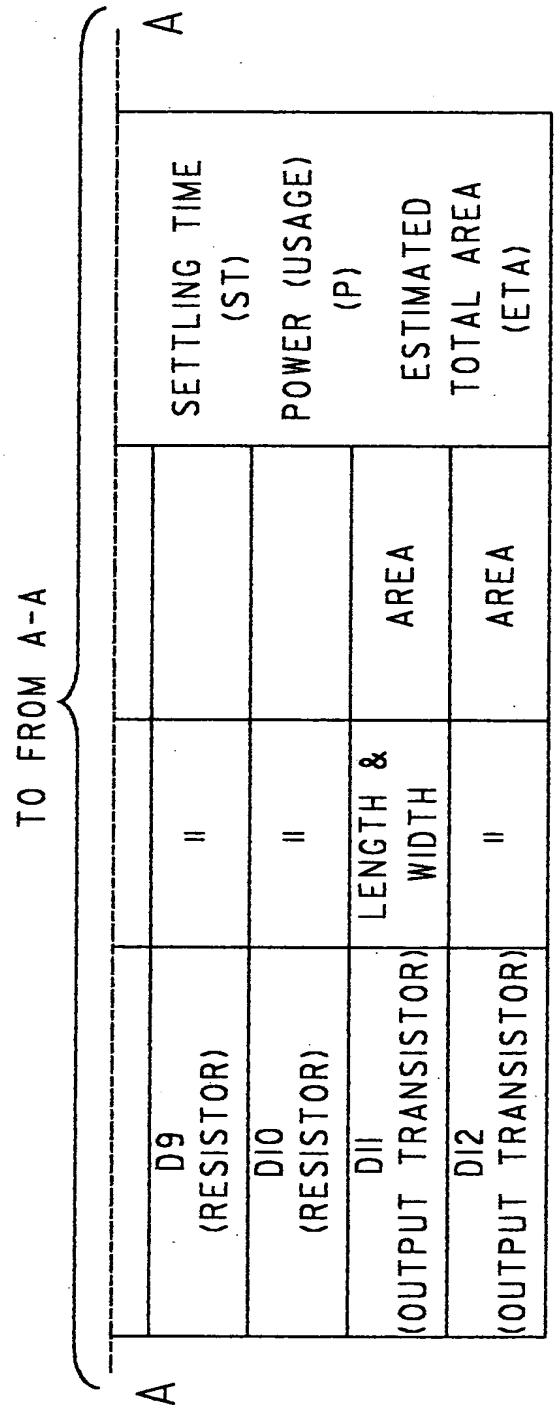


FIG. 1

FIG. 2


DEVICE(S)
DEVICE #
DEVICE VARIABLE(S)
DEVICE CONSTANTS(S)
SYNTHESIZED PERFORMANCE SPECIFICATION(S) *
D1 (INPUT TRANSISTOR)
D2 (INPUT TRANSISTOR)
D3 (INPUT TRANSISTOR)
D4 (RESISTOR)
D5 (CAPACITOR)
D6 (RESISTOR)
D7 (CAPACITOR)
D8 (RESISTOR)
LENGTH & WIDTH
=
=
RESISTANCE
CAPACITANCE
=
=
=
RESISTANCE
AREA
=
=
LENGTH & WIDTH
=
=
=
GAIN (G)
SLEW RATE (SR)
UNITY GAIN FREQ (UGF)
INPUT OFFSET (IO)
PHASE MARGIN (PM)
A
A
TO FROM A-A
8
10
6



* PERFORMANCE SPECIFICATIONS TO BE COMPARED TO CIRCUIT PERFORMANCES DETERMINED BY A CIRCUIT SYNTHESIZER

FIG. 2

FIG. 3

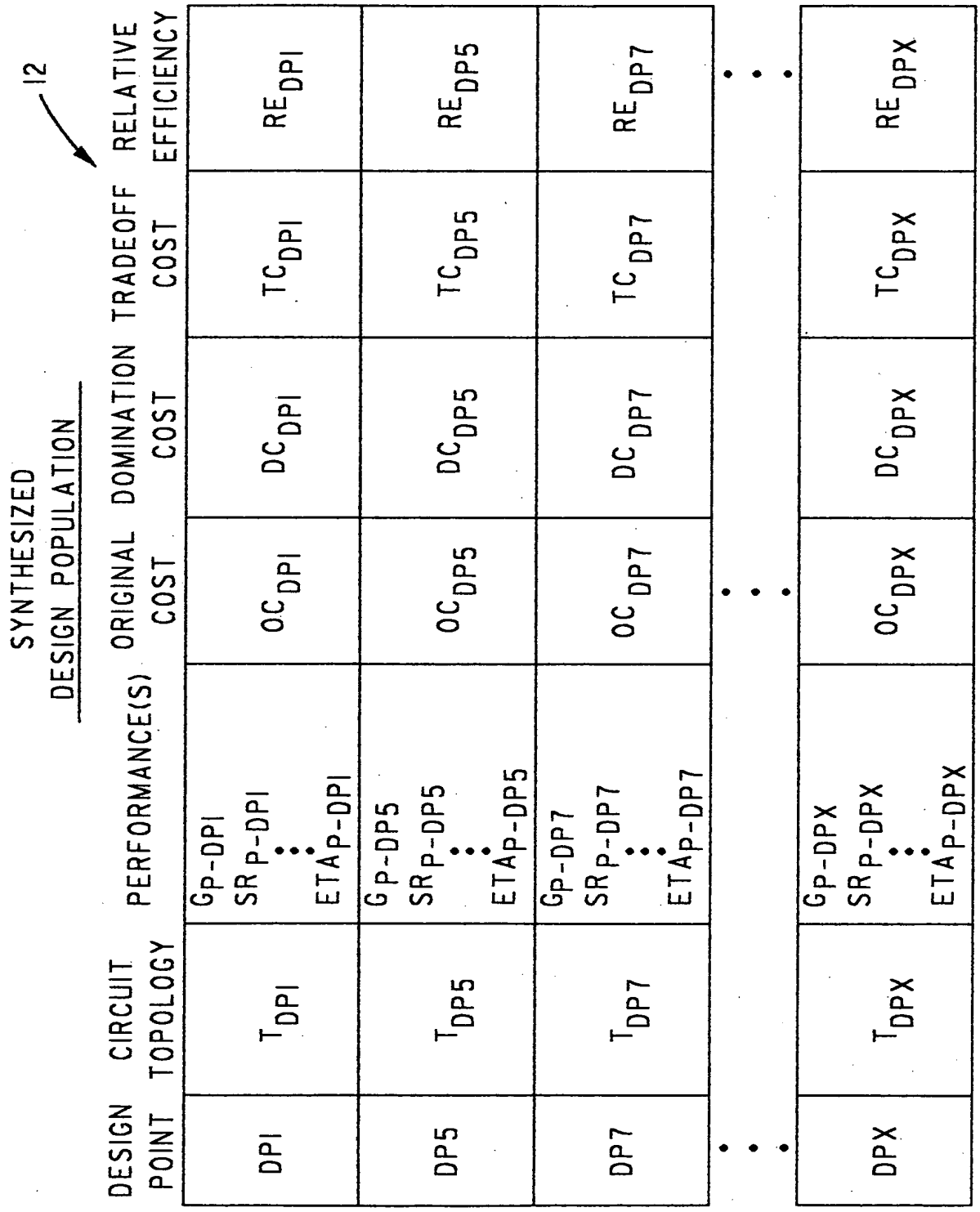

12
SYNTHESIZED DESIGN POPULATION
DESIGN POINT
CIRCUIT TOPOLOGY
PERFORMANCE(S)
ORIGINAL COST
DOMINATION COST
TRADEOFF COST
RELATIVE EFFICIENCY
DPI
T_{DPI}
G_{P-DPI} SR_{P-DPI} ... ETA_{P-DPI}
OC_{DPI}
DC_{DPI}
TC_{DPI}
RE_{DPI}
DP5
T_{DP5}
G_{P-DP5} SR_{P-DP5} ... ETA_{P-DP5}
OC_{DP5}
DC_{DP5}
TC_{DP5}
RE_{DP5}
DP7
T_{DP7}
G_{P-DP7} SR_{P-DP7} ... ETA_{P-DP7}
OC_{DP7}
DC_{DP7}
TC_{DP7}
RE_{DP7}
DPX
T_{DPX}
G_{P-DPX} SR_{P-DPX} ... ETA_{P-DPX}
OC_{DPX}
DC_{DPX}
TC_{DPX}
RE_{DPX}

FIG. 4

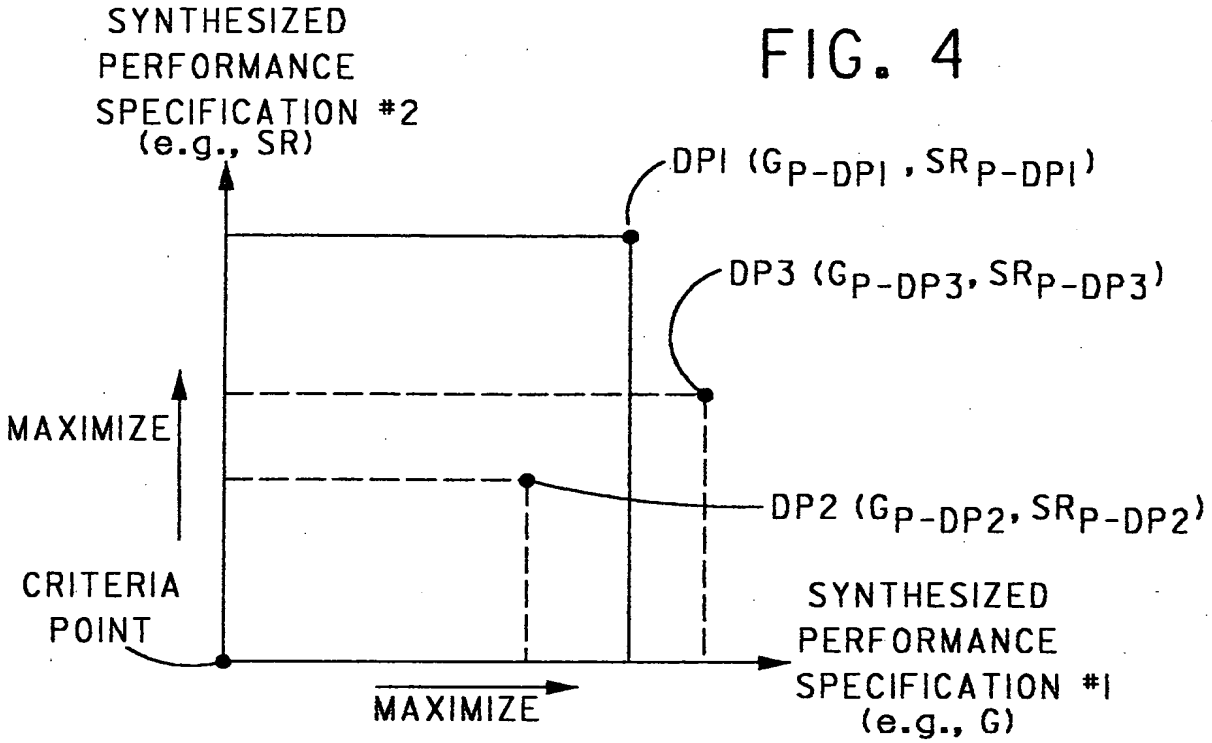
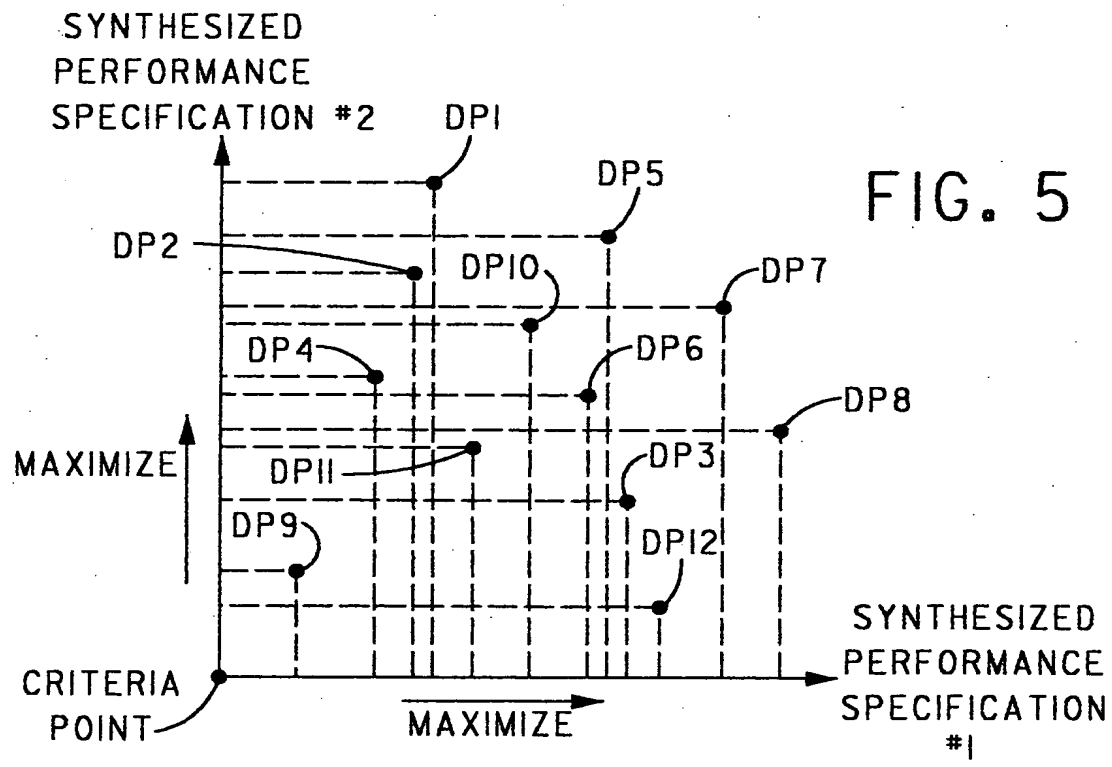

SYNTHESIZED PERFORMANCE SPECIFICATION #2 (e.g., SR)
DPI (G_{P-DPI}, SR_{P-DPI})
DP3 (G_{P-DP3}, SR_{P-DP3})
DP2 (G_{P-DP2}, SR_{P-DP2})
MAXIMIZE
CRITERIA POINT
MAXIMIZE
SYNTHESIZED PERFORMANCE SPECIFICATION #1 (e.g., G)

FIG. 5


SYNTHESIZED PERFORMANCE SPECIFICATION #2
DPI
DP5
DP2
DP10
DP7
DP4
DP6
DP8
MAXIMIZE
DP11
DP3
DP9
DP12
CRITERIA POINT
MAXIMIZE
SYNTHESIZED PERFORMANCE SPECIFICATION #1

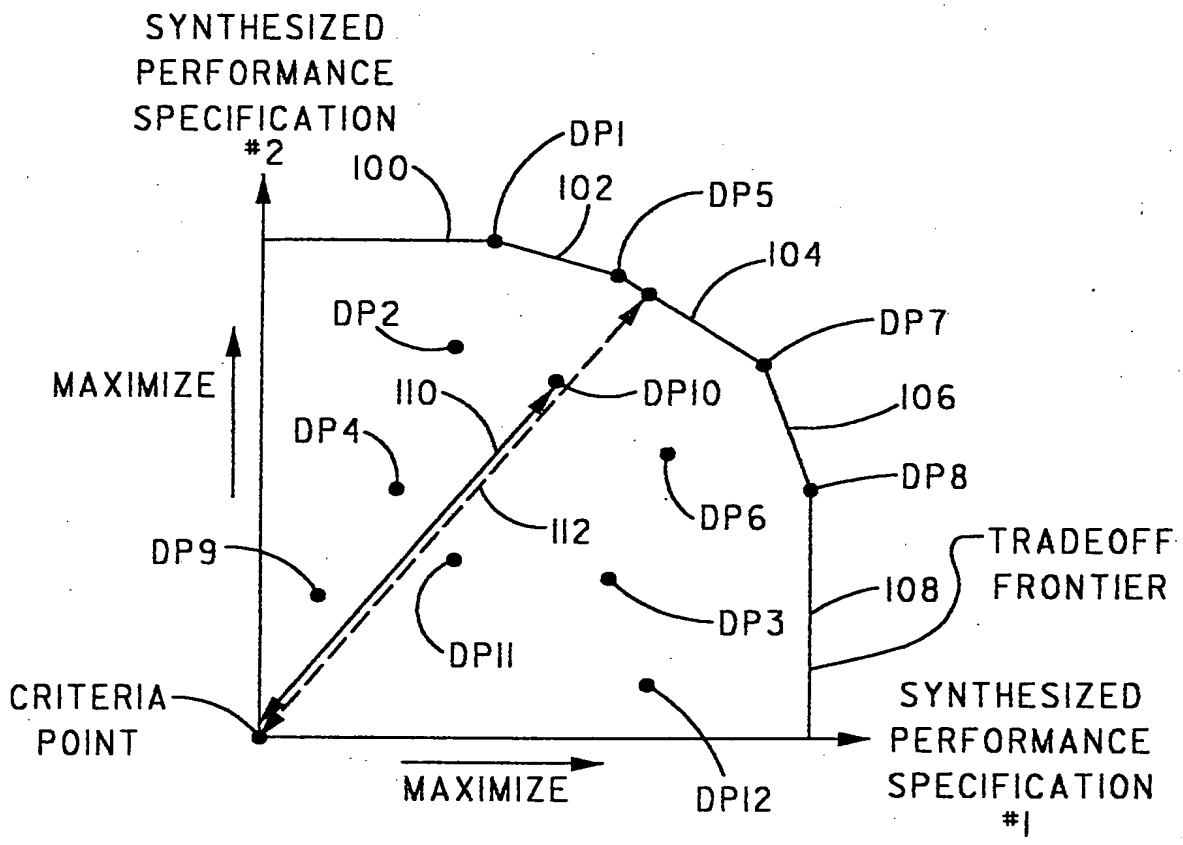
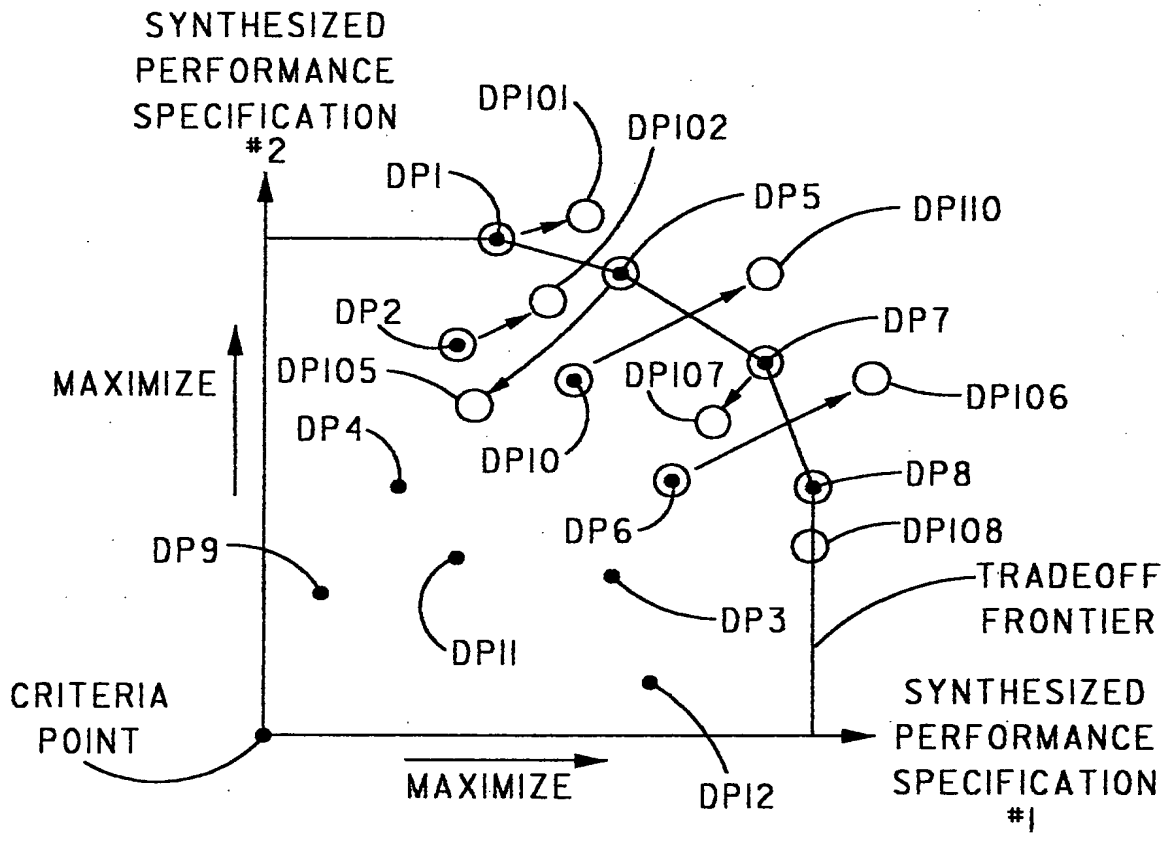

SYNTHESIZED PERFORMANCE SPECIFICATION #2
MAXIMIZE
CRITERIA POINT
MAXIMIZE
SYNTHESIZED PERFORMANCE SPECIFICATION #1
TRADEOFF FRONTIER
100
102
104
106
108
110
112
DP1
DP2
DP3
DP4
DP5
DP6
DP7
DP8
DP9
DP10
DP11
DP12

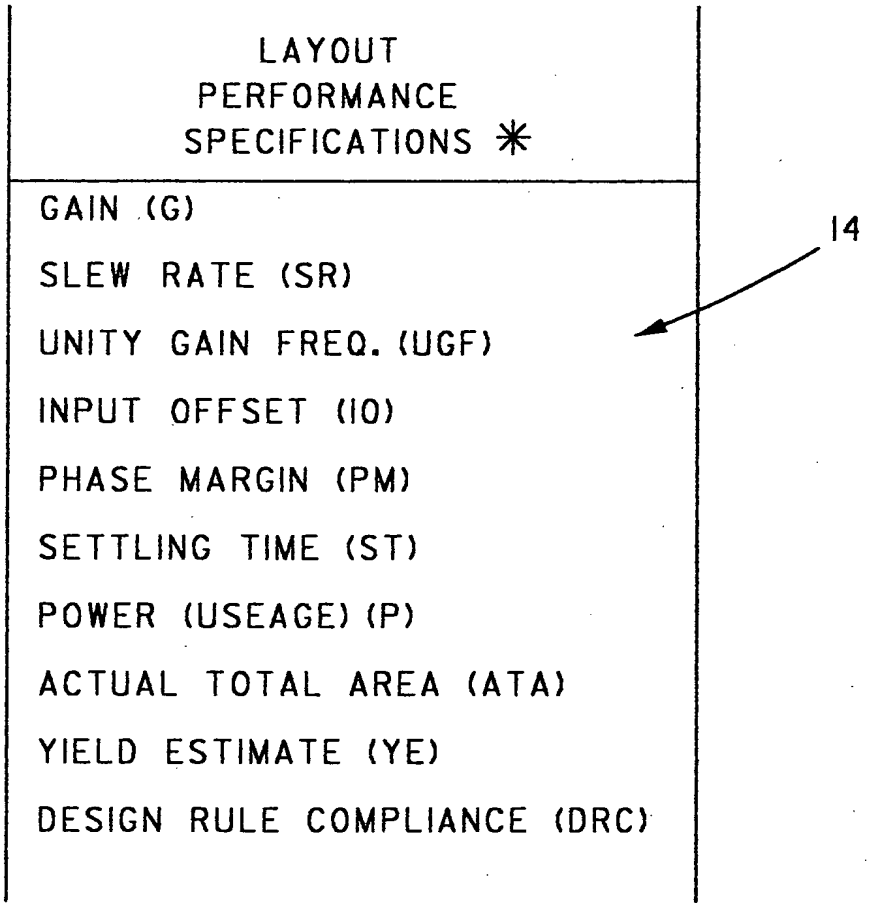
FIG. 6



◉ = DESIGN POINTS WITH LOWEST TRADEOFF COST

○ = NEW DESIGN POINTS GENERATED FROM DESIGN POINTS WITH LOWEST TRADEOFF COSTS

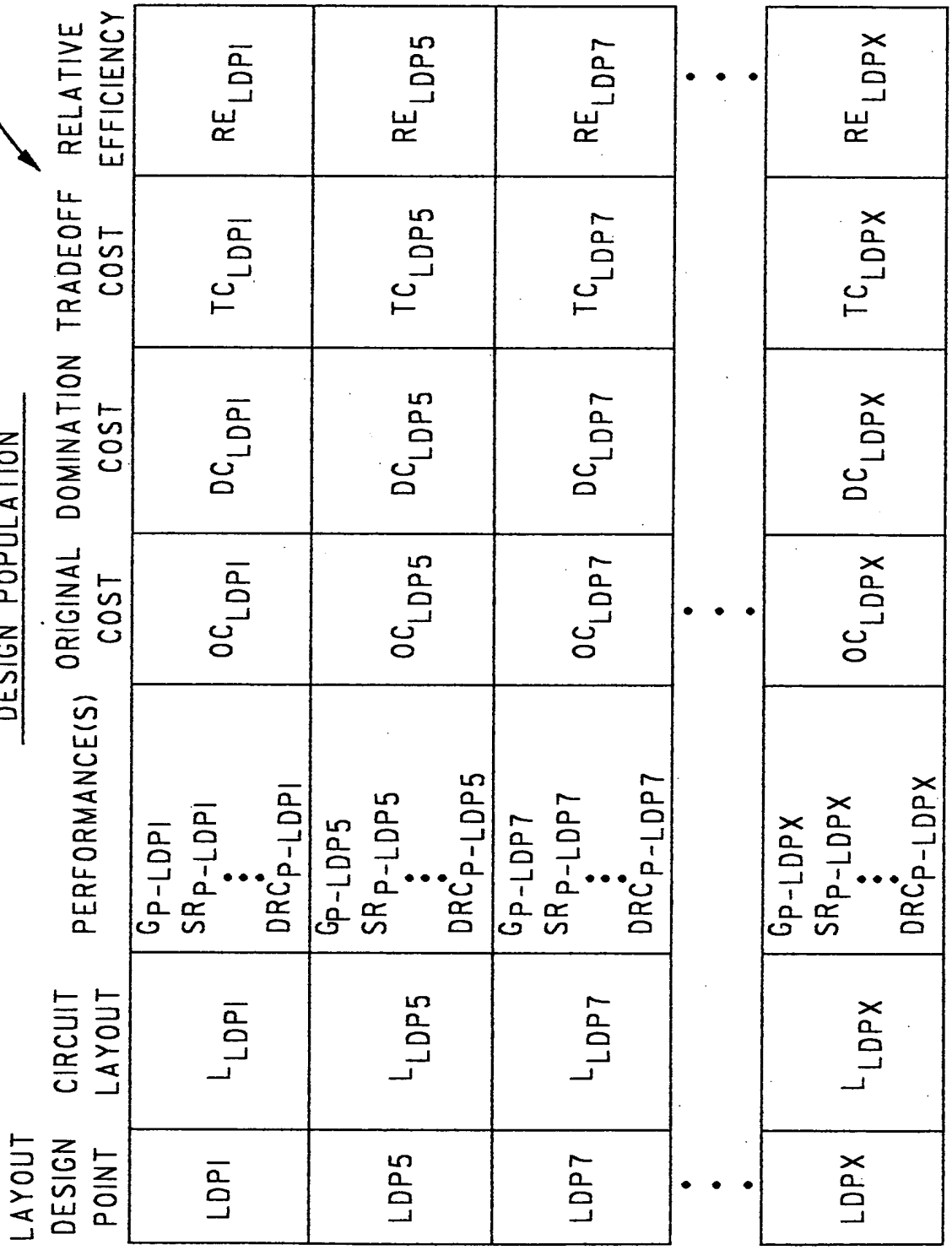
FIG. 7

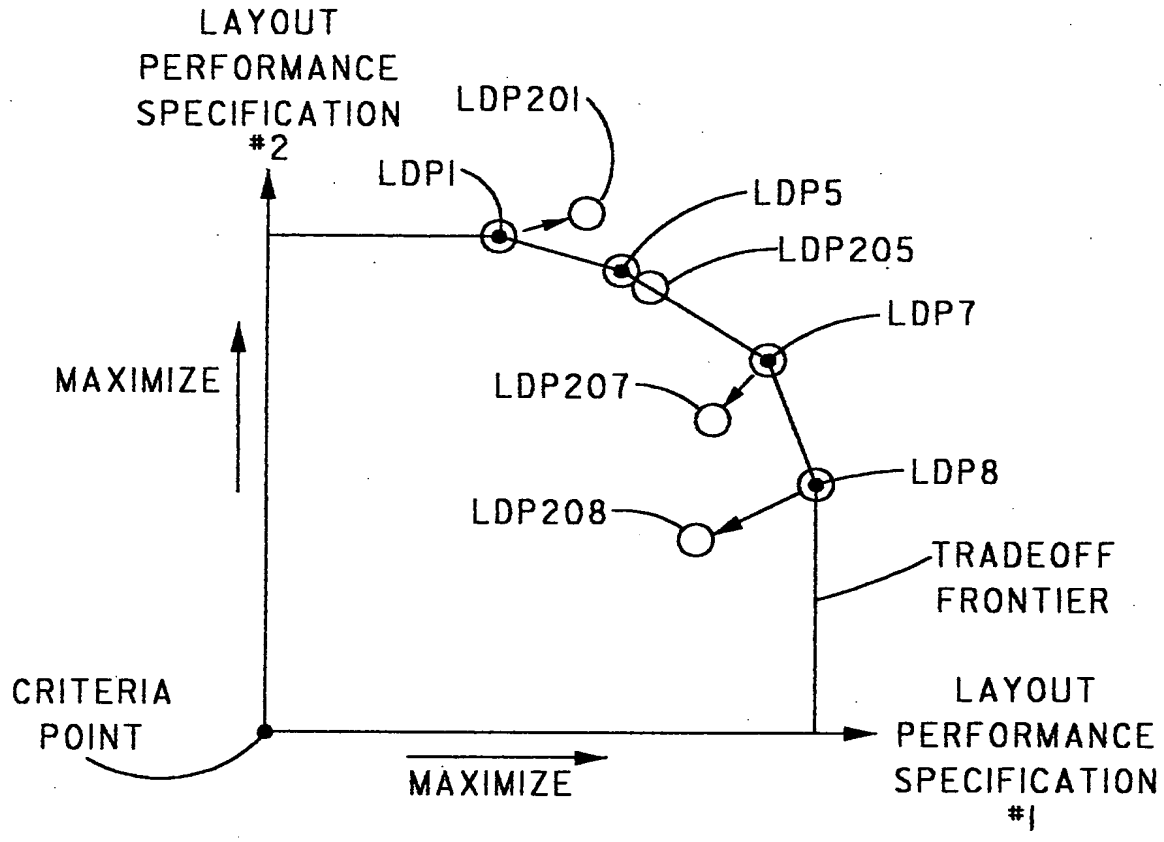


✳ PERFORMANCE SPECIFICATIONS TO BE COMPARED TO CIRCUIT PERFORMANCES DETERMINED BY A CIRCUIT SIMULATOR.

FIG. 8

FIG. 9


16
LAYOUT DESIGN POPULATION
LAYOUT DESIGN POINT
CIRCUIT LAYOUT
PERFORMANCE(S)
ORIGINAL COST
DOMINATION COST
TRADEOFF COST
RELATIVE EFFICIENCY
LDP1
LDP5
LDP7
LDPX
L_{LDP1}
L_{LDP5}
L_{LDP7}
L_{LDPX}
$G_{P\text{-}LDP1}$
$SR_{P\text{-}LDP1}$
$DRC_{P\text{-}LDP1}$
$G_{P\text{-}LDP5}$
$SR_{P\text{-}LDP5}$
$DRC_{P\text{-}LDP5}$
$G_{P\text{-}LDP7}$
$SR_{P\text{-}LDP7}$
$DRC_{P\text{-}LDP7}$
$G_{P\text{-}LDPX}$
$SR_{P\text{-}LDPX}$
$DRC_{P\text{-}LDPX}$
OC_{LDP1}
OC_{LDP5}
OC_{LDP7}
OC_{LDPX}
DC_{LDP1}
DC_{LDP5}
DC_{LDP7}
DC_{LDPX}
TC_{LDP1}
TC_{LDP5}
TC_{LDP7}
TC_{LDPX}
RE_{LDP1}
RE_{LDP5}
RE_{LDP7}
RE_{LDPX}



◉ = LAYOUT DESIGN POINT GENERATED FROM DESIGN POINTS WITH LOWEST TRADEOFF COST

○ = NEW LAYOUT DESIGN POINT GENERATED FROM LAYOUT DESIGN POINTS GENERATED FROM DESIGN POINTS WITH LOWEST TRADEOFF COSTS

FIG. 10